Remarks

Claims 1-14 are pending.

In the Office Action, it is stated that the information disclosure statement of 9/30/05 fails to comply with 37 C.F.R. 1.98(a)(2). Specifically, the Office alleges that the application file does not contain a copy of EP 1033759 A1. With this Amendment, Applicant has attached a copy of EP 1033759 A1 and respectfully requests the Office consider this reference as it is believed to have been submitted previously.

In the Office Action, claims 1-9 and 11-14 are rejected under 35 USC 103(a) over Darwish et al. (USPN 5,688,725), hereinafter "Darwish," in view of Kocon et al. (USPN 6,351,009), hereinafter "Kocon"; and claim 10 is rejected under 35 USC 103(a) over Darwish in view of Kocon, and further in view of Mo (USPN 6,316,806). Applicant respectfully traverses these rejections for the reasons stated below.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." (MPEP 706.02(j)). In this case, Applicant submits that the Office fails to establish a *prima facie* case of obviousness for the reasons stated below.

With regard to claim 1, the claimed invention includes, *inter alia*, "the ruggedness regions being more heavily doped than the source regions." (Emphasis added). Applicant submits that the suggested combination does not disclose or suggest this

feature. Rather, Darwish discloses that "N^+ source region 112 would normally be highly doped with a dosage of from $1x10^{14}$ to $7x10^{15}$ cm^{-2}[, and] P+ contact region 114 could be doped from $1x10^{14}$ to $5x10^{15}$ cm^{-2}." (Col. 5, lines 50-53). That is, P+ contact region 114 of Darwish (identified by the Office as the ruggedness region) is less heavily (or at least not more heavily) doped than the N^+ source region 112 (identified by the Office as the source regions). Kocon does not overcome, *inter alia*, this deficiency of Darwish because Kocon does not disclose or suggest anything regarding the comparative dosage between N^+ source region 306 and P^+ body region 304. In view of the foregoing, the suggested combination of the cited prior art references does not teach or suggest "the ruggedness regions being more heavily doped than the source regions." (Claim 1). As such, the Office fails to establish a *prima facie* case of obviousness. Accordingly, Applicant respectfully requests withdrawal of the rejection.

Applicant submits that the dependent claims are allowable for the same reasons stated above, as well as for their own additional features. For example, with regard to claim 11, the claimed invention includes, *inter alia*, "the doping concentration of the ruggedness regions is approximately 10 times than the doping concentration of the source regions." Admitting that Darwish and Kocon do not disclose this feature, the Office asserts that "it would have been obvious to one of ordinary skill in the art ... to have the doping concentration of the ruggedness regions being approximately 10 times greater than the doping concentration of the source regions," because "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the doping concentration of the ruggedness regions and the source regions[.]" (Office Action at pages 3-4). Applicant respectfully traverses this assertion because mere

possibility of modification is not enough to warrant a section 103 rejection. The Office must show a suggestion or motivation to modify the prior art. In this case, the Office fails to establish such a suggestion or motivation. The above-identified feature of the claimed invention is created based on, *inter alia*, a novel finding that "a significantly improved suppression of parasitic bipolar transistor action is achieved if the ruggedness regions are more heavily doped than the source regions[.]" (Specification of the claimed invention at page 5). Neither Darwish nor Kocon suggests such a motivation to improve suppression of parasitic bipolar transistor action. As such, neither Darwish nor Kocon suggests the ruggedness regions are more heavily doped than the source regions. Please note, it is not enough to show a motivation "to optimize the performance of a semiconductor device" (Office Action at page 4), rather, the Office needs to establish an artisan in the art is motivated to "optimize" the performance of "[a] vertical power transistor trench-gate semiconductor device" in the exact manner as disclosed in the claimed invention by the above-identified feature of claim 11. Applicant submits that the Office fails to establish this and the Office obtains a suggestion or motivation to modify only from the hindsight teachings of the claimed invention.

Applicant further submits that the factual assertion of the Office is not properly based upon common knowledge. For example, Applicant submits that even if, for sake of argument only, "it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the doping concentration of the ruggedness regions and the source regions[,]" one of ordinary skill in the art may not necessarily have the doping concentration of the ruggedness regions being approximately 10 times greater than the doping concentration of the source region. Accordingly,

Applicant respectfully requests that the Office support the findings with references that show these features. In view of the foregoing, the Office fails to establish a *prima facie* case of obviousness. Accordingly, Applicant respectfully requests withdrawal of the rejection.

Applicant respectfully submits that the application is in condition for allowance. If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

Dated: 2/21/06

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(54) MOS-gated device having a buried gate and process for forming same

(57) An improved trench MOS-gated device comprises a monocrystalline semiconductor substrate on which is disposed a doped upper layer. The upper layer includes at an upper surface a plurality of heavily doped body regions having a first polarity and overlying a drain region. The upper layer further includes at its upper surface a plurality of heavily doped source regions having a second polarity opposite that of the body regions A gate trench extends from the upper surface of the upper layer to the drain region and separates one source region from another. The trench has a floor and sidewalls comprising a layer of dielectric material and contains a conductive gate material filled to a selected level and an isolation layer of dielectric material that overlies the gate material and substantially fills the trench. The upper surface of the overlying layer of dielectric material in the trench is thus substantially coplanar with the upper surface of the upper layer. A process for forming an improved MOS-gate device provides a device whose gate trench is filled to a selected level with a conductive gate material, over which is formed an isolation dielectric layer whose upper surface is substantially coplanar with the upper surface of the upper layer of the device.

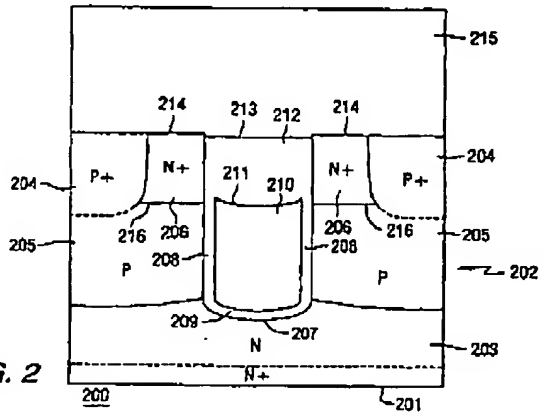

FIG. 2

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Description

[0001] The present invention relates to semiconductor devices and, more particularly, to an MOS-gated device and a process for forming same.

[0002] An MOS transistor that includes a trench gate structure offers important advantages over a planar transistor for high current, low voltage switching applications. In the latter configuration, constriction occurs at high current flows, an effect that places substantial constraints on the design of a transistor intended for operation under such conditions.

[0003] A trench gate of a DMOS device typically includes a trench extending from the source to the drain and having sidewalls and a floor that are each lined with a layer of thermally grown silicon dioxide. The lined trench is filled with doped polysilicon. The structure of the trench gate allows less constricted current flow and, consequently, provides lower values of specific on-resistance. Furthermore, the trench gate makes possible a decreased cell pitch in an MOS channel extending along the vertical sidewalls of the trench from the bottom of the source across the body of the transistor to the drain below. Channel density is thereby increased, which reduces the contribution of the channel to on-resistance. The structure and performance of trench DMOS transistors are discussed in Bulucea and Rossen, "Trench DMOS Transistor Technology for High-Current (100 A Range) Switching," in Solid-State Electronics, 1991, Vol. 34, No. 5, pp 493-507, the disclosure of which is incorporated herein by reference. In addition to their utility in DMOS devices, trench gates are also advantageously employed in insulated gate bipolar transistors (IGBTs), MOS-controlled thyristors (MCTs), and other MOS-gated devices.

[0004] FIG. 1 schematically depicts the cross-section of a trench MOS gate device 100 of the prior art. Although FIG. 1 shows only one MOSFET, a typical device currently employed in the industry consists of an array of MOSFETs arranged in various cellular or stripe layouts.

[0005] Device 100 includes a doped (depicted as N+) substrate 101 on which is grown a doped epitaxial layer 102. Epitaxial layer 102 includes drain region 103, heavily doped (P+) body regions 104, and P-wells 105. Abutting body regions in epitaxial layer 103 are heavily doped (N+) source regions 106, which are separated from each other by a gate trench107 that has dielectric sidewalls 108 and floor 109. Gate trench 107 is substantially filled with gate semiconductor material 110. Because the source regions 106 and gate semiconductor material 110 have to be electrically isolated for device 100 to function, they are covered by a dielectric layer 111. Contact openings 112 enable metal 113 to contact body regions 104 and source regions 106.

[0006] Contact openings 112 are formed in dielectric layer 111, which typically is a deposited layer of oxide, by conventional mask/etch techniques. The size of device 100 depends on the minimum thickness of dielectric needed for isolation (the lateral distance between a source region 106 and gate trench 107) and on the tolerance capabilities of the mask/etch procedures. The thickness of dielectric layer 111 is determined not only by the minimum required voltage isolation but also on the need to minimize source-to-gate capacitance, which effects device switching speed and switching losses. Switching losses are directly proportional to the capacitance, which is in turn inversely proportional to the dielectric thickness. Therefore there is a typical minimum thickness of about 0.5-0.8 μm for dielectric layer 111 in prior art device 100.

[0007] As just noted, the required minimum thickness of dielectric layer 111 imposes limitations on the minimum size of device 100. It would be desirable to be able to reduce the size and improve the efficiency of semiconductor devices. The present invention provides these benefits.

[0008] The present invention includes a trench MOS-gated device comprising a substrate comprising doped monocrystalline semiconductor material, a doped upper layer disposed on said substrate, said upper layer having an upper surface and comprising at said upper surface a plurality of heavily doped body regions having a first polarity, said body regions overlying a drain region in said upper layer, said upper layer further comprising at said upper surface a plurality of heavily doped source regions having a second polarity and extending from said upper surface to a selected depth in said upper layer, a gate trench separating one of said source regions from a second source region, said trench extending from said upper surface of said upper layer to said drain region, said trench having a floor and sidewalls comprising a layer of dielectric material, said trench being filled with a conductive gate material to a selected level substantially below the upper surface of the upper layer and with an isolation layer of dielectric material overlying said gate material, said overlying layer of dielectric material in said trench having an upper surface that is substantially coplanar with said upper surface of said upper layer, in which the substrate comprises monocrystalline silicon, and upper layer comprises an epitaxial layer.

[0009] The invention also includes a process for forming a trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;
(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;
(c) forming a gate trench mask on said upper surface of said upper layer;
(d) forming a plurality of gate trenches extending from the upper surface of said upper layer through

said well region to said drain region;

(e) forming sidewalls and floor each comprising a dielectric material in each of said gate trenches;

(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material;

(g) removing said trench mask from the upper surface of said upper layer;

(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;

(i) removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is substantially coplanar with the upper surface of said upper layer;

(j) forming a plurality of heavily doped source regions having a second polarity in said body regions, said source regions extending to a selected depth from the upper surface of said upper layer;

(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer; and

(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.

(m) said substrate preferably comprises monocrystalline silicon, and said upper layer comprises an epitaxial layer.

[0010] Conveniently, the present invention is directed to a trench MOS-gated device formed on a monocrystalline semiconductor substrate comprising a doped upper layer. The doped upper layer, includes at an upper surface a plurality of heavily doped body regions having a first polarity and overlying a well region and a drain region. The upper layer further includes at its upper surface a plurality of heavily doped source regions that have a second polarity opposite that of the body regions and extend to a selected depth in the upper layer.

[0011] A gate trench extends from the upper surface of the upper layer through the well region to the drain region and separates one source region from a second source region. The trench has a floor and sidewalls comprising a layer of dielectric material and contains a conductive gate material filling the trench to a selected level and an isolation layer of dielectric material that overlies the gate material and substantially fills the trench. The upper surface of the overlying layer of dielectric material in the trench is thus substantially coplanar with the upper surface of the upper layer.

[0012] Advantageously, a process for forming a high density, self-aligned trench MOS-gated device. A doped upper layer having an upper surface and an underlying drain region is formed on a substrate, and a well region having a first polarity is formed in the upper layer over the drain region. A gate trench mask is formed on the upper surface of the upper layer, and a plurality of gate trenches extending from the upper surface through the well region to the drain region are etched in the upper layer.

[0013] Sidewalls and a floor each comprising a dielectric material are formed in each of the gate trenches, which are filled to a selected level with a conductive gate material. The trench mask is removed, and an isolation layer of dielectric material is formed on the top surface of the upper layer and within the gate trench, where it overlies the gate material and substantially fills the trench. The dielectric layer is removed from the top surface of the upper layer; the dielectric layer remaining within the trench has an upper surface that is substantially coplanar with the upper surface of the upper layer.

[0014] A plurality of heavily doped body regions having a first polarity are formed at the upper surface of the upper layer. A source mask is formed on the upper surface, and a plurality of heavily doped source regions having a second polarity and extending to a selected depth into the upper layer are formed in the body regions. Following removal of the source mask, a metal contact to said body and source regions is formed over the upper surface of the upper layer.

[0015] The invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIG. 1 schematically depicts a cross-section of a trench MOS-gated device 100 of the prior art.

FIG. 2 is a schematic cross-sectional representation of a trench MOS-gated device 200 of the present invention; FIGS. 2A-D illustrate the process of forming device 200.

FIGS. 3A and 3B schematically depict cross-sections of another device 300 in accordance with the present invention; FIG. 3C is a schematic plan view of device 300.

[0016] The trench MOS-gated device, by eliminating the surface area required for gate-source dielectric isolation, enables the size of the device to be substantially reduced. A masking procedure to form contact openings in the dielectric layer is also avoided; the gate trench is thus self-aligned.

[0017] FIG. 2 depicts an improved trench MOS-gated device 200. The device 200 includes a doped N+ substrate 201 on which is deposited an epitaxial doped upper layer 202. Epitaxial layer 202 includes drain region 203, heavily doped P+ body regions 204, and P- well regions 205. Abutting body regions 204 in epitaxial layer 203 are heavily doped N+ source regions 206, which are separated from each other by a gate trench 207 that has dielectric sidewalls 208 and floor 209. Contained within trench 207 is a gate material 210, filled to a selected level 211, and an overlying dielectric layer

212. Selected level 211 of gate material 210 is approximately coplanar with the selected depth 216 of N+ source regions 206, thereby providing overlap between source regions 206 and gate material 210. The surface 213 of gate dielectric layer 212 is substantially coplanar with the surface 214 of epitaxial layer 202. Deposited metal layer 215 is able to contact body regions 204 and source regions 206 without the need for a masking procedure to form contact openings.

[0018] Because gate material 210 is recessed within gate trench 207 to permit the inclusion of dielectric layer 212 of sufficient thickness to provide gate isolation, diffusions to form N+ source regions 206 must be deep enough to ensure overlap with gate material 210. Although source regions 206 are shown as having N polarity and body regions 204 are depicted as having P polarity in device 200, it is understood that the polarities of these regions can be reversed from those shown in FIG. 2.

[0019] FIGS. 2A-D schematically illustrate the process of forming device 200. As shown in FIG. 2A, on a doped semiconductor substrate 201, which can be monocrystalline silicon, is formed a doped upper layer 202 that includes a drain region 203. Upper layer 202 can be epitaxially grown silicon or, for lower voltage devices (ca 12V), a heavily doped portion of substrate 201. P well regions 205 are formed in layer 202 by doping into upper layer surface 214. A trench mask TM patterned to define a gate trench is formed on surface 214, and gate trench 207 extending through P-well regions 205 to drain region 203 is etched in layer 202. Trench dielectric sidewalls 208 and floor 209, preferably comprising silicon dioxide, which can be either deposited or grown, are formed in gate trench 207, which is then filled with a conductive gate material 210, which can be, for example, a metal, a silicide or doped polysilicon, to a selected depth 211.

[0020] Referring to FIG. 2B, following removal of trench mask TM, filling of trench 207 is completed by forming an isolation dielectric layer 212, which can be silicon dioxide, over gate material 210 in trench 20 and on surface 214. A planarization dielectric etch is performed to re-expose surface 214 without removing dielectric material 212 from trench 207. Surface 213 of dielectric layer 212 in trench 207 is thereby rendered substantially coplanar with upper surface 214 of layer 202. It may be advantageous, however, to etch surface 213 slightly below surface 214 in order to increase source contact and improve device on-resistance characteristics.

[0021] Also as shown in FIG. 2B, N+ source regions 206 are formed in layer 202 by ion implantation and diffusion to a selected depth 216 that is approximately coplanar with selected level 211 of dielectric material 210 and thereby provides overlap between gate material 210 and source regions 206.

[0022] Referring to FIG. 2C, a body mask M is formed on surface 214, and P+ body regions 204 are formed by further doping of layer 202. Removal of the body mask M, followed by deposition of metal 215 to provide contact with body regions 204 and source regions 206, completes the formation of device 200, as shown in FIG. 2D. Metal (not shown) can be deposited on the reverse side of the substrate to provide contact with drain region 203. Although in the just described fabrication sequence, the formation of source regions 206 preceded the formation of body regions 204, it is recognized that this ordering is not critical and that the described masking procedure can be varied for the purpose of convenience.

[0023] Gate trenches 207 included in a device of the present invention may have an open-cell stripe topology or a closed-cell cellular topology. Furthermore, in the closed- cell cellular topology, the trenches may have a square or, more preferably, a hexagonal configuration. Although device 200, as schematically depicted in FIG. 2, is a power MOSFET, the present invention is applicable to the construction of other MOS-gated devices such as an insulated gate bipolar transistor (IGBT), an MOS-controlled thyristor (MCT), and an accumulation field effect transistor (ACCUFET).

[0024] FIGS. 3A-C depict an alternative embodiment of the present invention. Device 300 includes a doped N+ substrate 301, on which is disposed a doped upper layer 302. Upper layer 302 includes drain region 303 and P-wells 305. As shown in FIG. 3A, P+ body regions 304 are formed in layer 302 and separated from each other by a gate trench 307. Similarly, as depicted in FIG. 3B, N+ source regions 306, formed by ion implantation and diffusion to a selected depth 316 in upper layer 302, are also separated by gate trench 307. Gate trenches 307 each have dielectric sidewalls 308 and a floor 309 and contain conductive gate material 310, filled to a selected level 311, and an overlying dielectric layer 312. The surface 313 of gate dielectric layer 312 is substantially coplanar with the surface 314 of upper layer 302. Metal layer 315 is deposited on surface 314 to contact body regions 304 and source regions 306.

[0025] As shown in FIG. 3C, device 300 includes a plurality of arrays 317 of alternating P+ body regions 304 and N+ source regions 306. Each array 317 is disposed adjacent to a gate trench 307 and separated from a second array 317 by the gate trench 307. Also, as depicted in FIG. 3C, source regions 306 comprise a greater portion, body regions 304 a lesser portion, of the lengthwise dimension of an array 317 disposed alongside a gate trench 307.

[0026] In the formation of device 300, following the planarization of dielectric layer 312 to re-expose surface 314, P+ body regions are formed in upper layer 302 by doping. A non-critical source mask (not shown), disposed transversely to trenches 307, is formed on surface 314, and source regions 306 are formed by ion implantation and diffusion. The arrangement of body regions 304 and source regions 306 in arrays 317 sep-

arated by gate trenches 307, as depicted for device 300 in FIGS. 3A-C, further exploits the advantage of device size reduction.

[0027] An improved trench MOS-gated device comprises a monocrystalline semiconductor substrate on which is disposed a doped upper layer. The upper layer includes at an upper surface a plurality of heavily doped body regions having a first polarity and overlying a drain region. The upper layer further includes at its upper surface a plurality of heavily doped source regions having a second polarity opposite that of the body regions A gate trench extends from the upper surface of the upper layer to the drain region and separates one source region from another. The trench has a floor and sidewalls comprising a layer of dielectric material and contains a conductive gate material filled to a selected level and an isolation layer of dielectric material that overlies the gate material and substantially fills the trench. The upper surface of the overlying layer of dielectric material in the trench is thus substantially coplanar with the upper surface of the upper layer. A process for forming an improved MOS-gate device provides a device whose gate trench is filled to a selected level with a conductive gate material, over which is formed an isolation dielectric layer whose upper surface is substantially coplanar with the upper surface of the upper layer of the device.

Claims

1. A trench MOS-gated device comprising a substrate comprising doped monocrystalline semiconductor material, a doped upper layer disposed on said substrate, said upper layer having an upper surface and comprising at said upper surface a plurality of heavily doped body regions having a first polarity, said body regions overlying a drain region in said upper layer, said upper layer further comprising at said upper surface a plurality of heavily doped source regions having a second polarity and extending from said upper surface to a selected depth in said upper layer, a gate trench separating one of said source regions from a second source region, said trench extending from said upper surface of said upper layer to said drain region, said trench having a floor and sidewalls comprising a layer of dielectric material, said trench being filled with a conductive gate material to a selected level substantially below the upper surface of the upper layer and with an isolation layer of dielectric material overlying said gate material, said overlying layer of dielectric material in said trench having an upper surface that is substantially coplanar with said upper surface of said upper layer, in which the substrate comprises monocrystalline silicon, and upper layer comprises an epitaxial layer.

2. A device as claimed in claim 1 wherein said upper layer comprises a well region having said first polarity, said well region underlying said body and source regions and overlying said drain region, and one of said source regions is disposed between and adjacent to one of said source regions and a gate trench, and preferably one of said source regions is disposed between and adjacent to two gate trenches.

3. A device as claimed in claim 1 wherein said plurality of body regions and said plurality of source regions comprise a plurality of arrays of alternating body regions and source regions each disposed adjacent to a gate trench, and wherein one of said arrays is separated from a second of said arrays by said gate trench, and each said array of alternating body regions and source regions have a lengthwise dimension along said gate trench, said source regions comprising a greater portion and said body regions comprising a lesser portion of said lengthwise dimension.

4. A device as claimed in claim 1 wherein the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer, in which said dielectric material forming said sidewalls, said floor, and said isolation layer in said gate trench comprises silicon dioxide.

5. A device as claimed in claim 4 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon, and said first polarization is P and said second polarization is N, or said first polarization is N and said second polarization is P.

6. A device as claimed in claim 1 comprising a plurality of gate trenches having an open-cell stripe topology, or a plurality of gate trenches having a closed-cell cellular topology, and in which cells in said closed-cell cellular topology have a square configuration or a hexagonal configuration.

7. A process for forming a trench MOS-gated device, said process comprising:

(a) forming a doped upper layer on a semiconductor substrate, said upper layer having an upper surface and an underlying drain region;
(b) forming a well region having a first polarity in said upper layer, said well region overlying said drain region;
(c) forming a gate trench mask on said upper surface of said upper layer;
(d) forming a plurality of gate trenches extending from the upper surface of said upper layer through said well region to said drain region;

(e) forming sidewalls and floor each comprising a dielectric material in each of said gate trenches;
(f) filling each of said gate trenches to a selected level substantially below the upper surface of said upper level with a conductive gate material;
(g) removing said trench mask from the upper surface of said upper layer;
(h) forming an isolation layer of dielectric material on the upper surface of said upper layer and within said gate trench, said isolation layer overlying said gate material and substantially filling said trench;
(i) removing said dielectric layer from the upper surface of said upper layer, said dielectric layer remaining within and substantially filling said trench having an upper surface that is substantially coplanar with the upper surface of said upper layer;
(j) forming a plurality of heavily doped source regions having a second polarity in said body regions, said source regions extending to a selected depth from the upper surface of said upper layer;
(k) forming a plurality of heavily doped body regions having a first polarity at the upper surface of said upper layer, said body regions overlying the drain region in said upper layer; and
(l) forming a metal contact to said body and source regions over the upper surface of said upper layer.
(m) said substrate preferably comprises monocrystalline silicon, and said upper layer comprises an epitaxial layer.

8. A process as claimed in claim 7 wherein said upper layer comprises a heavily doped portion of said substrate, with one of said source regions is disposed between and adjacent to one of said source regions and a gate trench.

9. A process as claimed in claim 8 wherein one of said source regions is disposed between and adjacent to two gate trenches, with said forming well region comprises doping said upper layer.

10. A process as claimed in claim 9 wherein said forming heavily doped body regions comprises further doping said upper layer, and said forming heavily doped source regions comprises masked ion implanting and diffusing, in which preferably said masked ion implanting and diffusing is to a selected depth in said doped layer that is substantially coplanar with said filling level of said gate material in said gate trench.

11. A process as claimed in claim 7 wherein the forming said source regions and said body regions comprises:

implanting the entire upper surface of said substrate with a ions of said second polarity, then forming a body mask on the upper surface of said substrate, said mask comprising openings transverse to said trenches;
doping the upper surface of said substrate with a dopant of said first polarity, then removing said body mask; said plurality of body regions and said plurality of source regions comprise a plurality of arrays of alternating body regions and source regions each disposed adjacent to a gate trench, and wherein one of said arrays is separated from a second of said arrays by said gate trench.

12. A process as claimed in claim 11 wherein each said array of alternating body regions and source regions have a lengthwise dimension along said gate trench, said source regions comprising a greater portion and said body regions comprising a lesser portion of said lengthwise dimension.

13. A process as claimed in claim 7 wherein said conductive gate material within said gate trench is selected from the group consisting of a metal, a silicide, and doped polysilicon, the selected level of gate material in the trench is substantially coplanar with the selected depth of the source regions in the upper layer, in which said first polarization is P and said second polarization is N, or said first polarization is N and said second polarization is P.

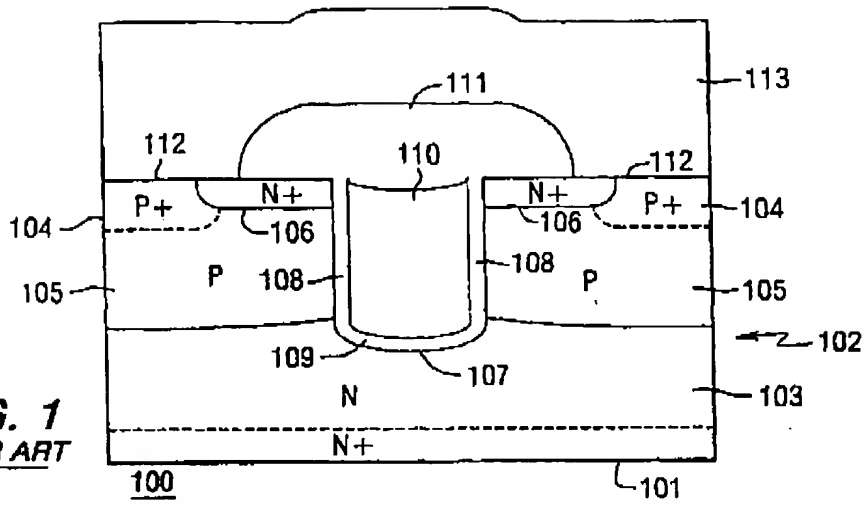


FIG. 1
PRIOR ART

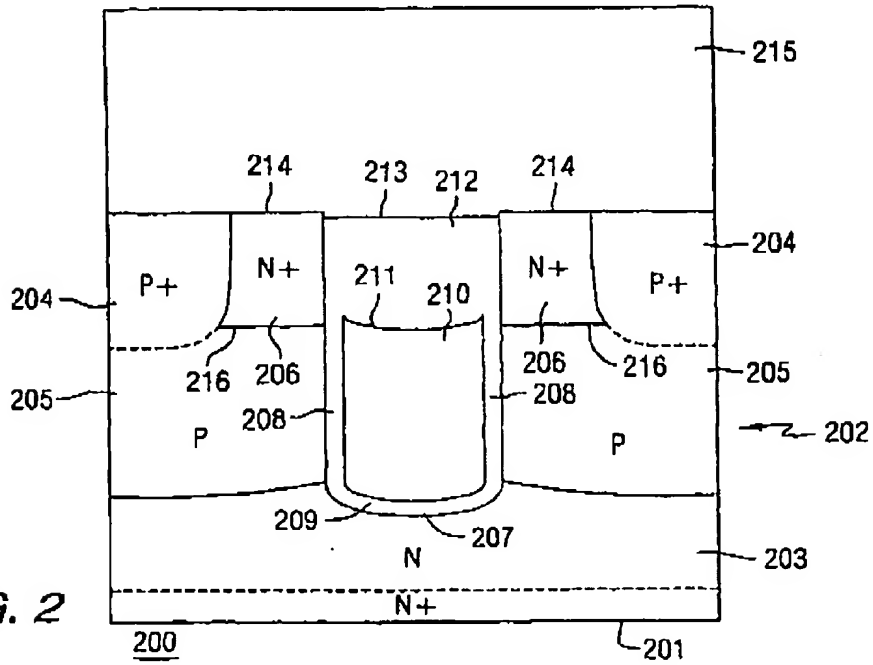
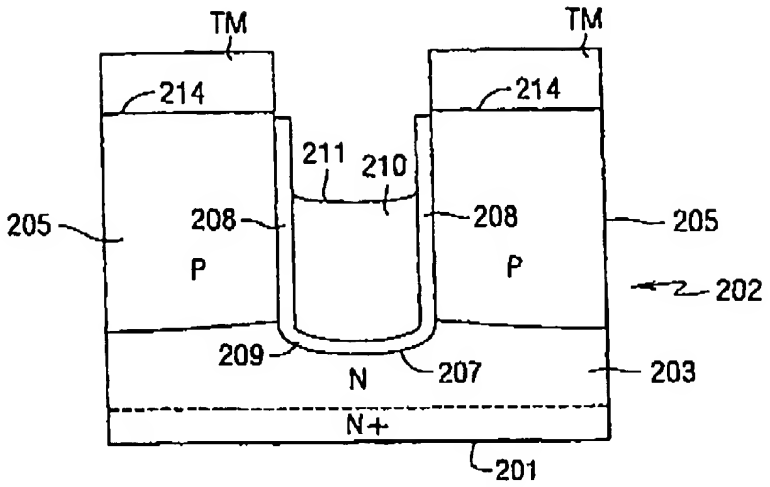


FIG. 2


TM
TM
214
214
211
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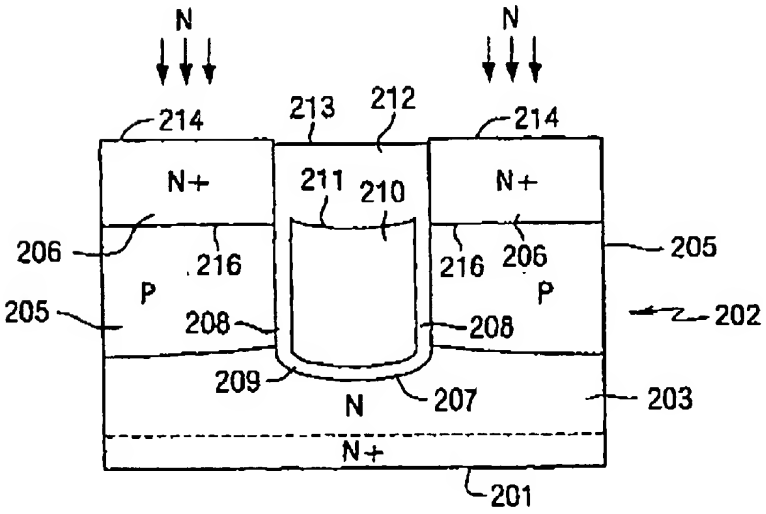
205
208
208
205
P
P
202
209
N
207
203
N+
201

FIG. 2A


N
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203
N+
201

FIG. 2B

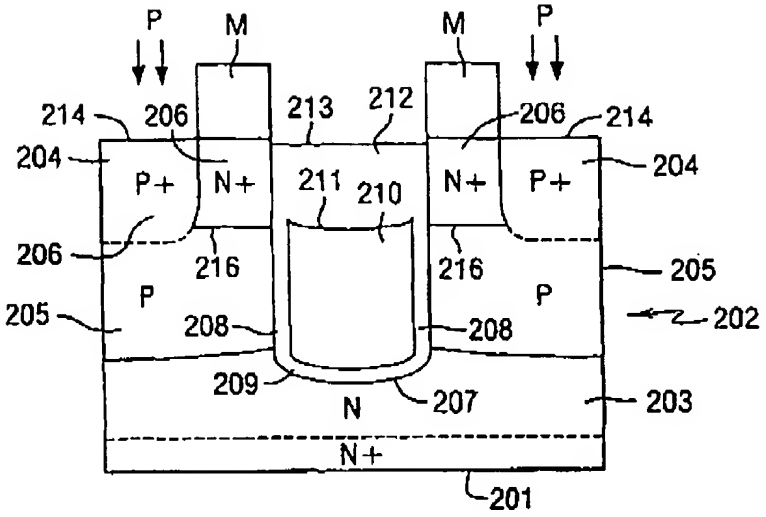
P
M
M
P
214
206
213
212
206
214
204
P+
N+
211
210
N+
P+
204
206
216
216
205
P
P
205
208
208
202
209
N
207
203
N+
201

FIG. 2C

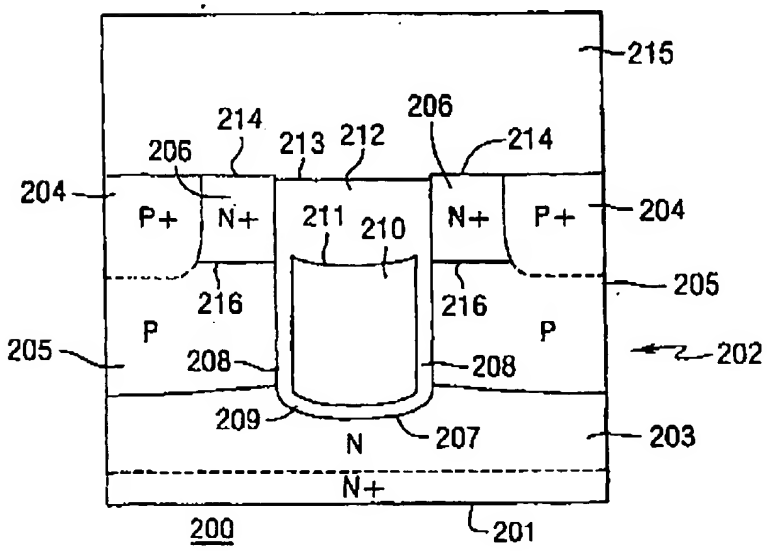
215
214
206
206
213
212
206
214
204
P+
N+
211
210
N+
P+
204
205
216
216
P
P
205
208
208
202
209
N
207
203
N+
200
201

FIG. 2D